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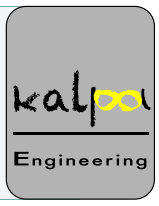

A New Symmetric Multilevel Voltage Source Inverter with Least Number of Switches

Malu D. Prajapati
Laljibhai Chaturbhai Institute of Technology.
Malu.prajapati92@gmail.com

Abstract

In this paper, a new symmetric multilevel voltage source inverter is proposed which consist less number of switches as compared to conventional multilevel inverter. This new symmetric MLI is able to produce desired value of voltage level with reduced number of switches. Also, multilevel inverter has good harmonic profile that is able to reduce total harmonic distortion without affecting desired output power. Moreover, in comparison with conventional cascade multilevel inverter, this new symmetric topology ultimately reduced the number of switches, the number of gate driver circuit, inverter cost, installation area and power loss due to reduced amount of on state switches.

1 Introduction

Recently, Inverters are accepted as a one part of renewable energy system that are able to convert DC input quantity in to AC output quantity. The reason behind concept is that output form of renewable energy system is in DC form while electrical transmission system is in AC form. Nowadays different types of application use multilevel inverter concept which was introduced by Nabae et al. Multilevel inverters are generally used in power system, static reactive power compensation, micro grid systems, adjustable speed drive etc. The basic configuration of multilevel inverters is diode clamped inverter, capacitor clamped inverter and cascaded inverter which are used to generate stepped waveform. Multilevel inverter consists different types of switching state depending upon required level of output. As compared to conventional 2 level inverter, multilevel inverter has various features like:

- Higher power quality
- Lower harmonic distortion
- Fundamental component consists good amplitude
- Higher efficiency
- Lower losses at switching frequency etc.

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These are the reason to use multilevel inverter instead of 2-level inverter. In the concept of multilevel inverter, if the number of levels are increased that will ultimately increase the circuit complexity which will effect on efficiency and reliability. Also in diode clamped inverter, voltage imbalance problem is happened and in flying capacitor floating capacitors are used to clamp the voltage level. While cascaded inverter consist array of H- bridge cell connected in series.

This paper proposed a new symmetric multilevel voltage source inverter which will generate more number of voltage level by using less number of IGBT power switches. If the number of switches are reduced that will reduce the number of gate driver circuit also. The use of less number of on state switches reduces power loss and voltage drop across it. Thus the cost and installation area are also less required. This topology can be implemented for asymmetric concept also.

The reminder of this paper is arranged as follows: Section 2 discusses the new symmetric inverter configuration. Section 3 illustrates the comparison between proposed inverter and other multilevel inverter. Section 4 illustrate the control strategy and switching state which are implemented for this proposed topology. Section 5 illustrates simulation results. In last, Section 6 represents conclusion. .

2 Proposed Topology

Generally, in multilevel configuration, it is necessary to select required number of component depends on the number of output voltage level. Thus the number of components are increased to generate high level of output voltage which will increase the cost, installation area and switches. Thus this topology in introduced to reduce the number of switches for higher order of output voltage level.

"Fig.1," shows the basic concept of a new symmetric multilevel voltage source inverter. The proposed topology consists connection of H-bridge with six power switches in a proper way. This connection provides stepped output waveform with polarity. The word symmetric indicate that required DC voltage source have equal value. Each cell consists of two power switches with one DC source. The power switches consist of an IGBT with anti-parallel fast recovery diode. The DC voltage source can be achieved by using transformers and rectifier. Rectifier are connected with transformer which are fed from AC line and produce DC voltage source. The output voltage is the sum of all DC input voltage. So the total output voltage can be calculated by using this equation:

$$V_{o,max} = \sum_{i=1}^{n} V_i = nV_{dc} \qquad (1)$$

Where, n is the number of DC sources

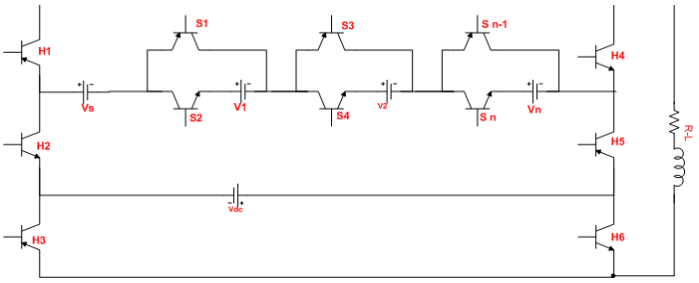

Figure 1: Proposed symmetric inverter

The value of DC source can be considered either zero or V_{dc}.

To generate m-levels in the output voltage, n-DC voltage sources are required.

$$n = \frac{m-1}{2} \quad (2)$$

Where, m is the number of levels in output voltage

For example, four DC voltage sources are required to obtain 9-levels in the output voltage and five DC voltage sources are required to generate 11-levels in the output voltage.

When switches are changed their states from on to off or off to on, a small amount of voltage drop will be produced. So the power loss calculation is introduced. In symmetric topology, (n+1) switches are conducted during every step of voltage level. While in asymmetric topology, (n+2) switches are conducted during every step of voltage level. Finally, the calculation of total output voltage including voltage drop can be calculated as:

$$V_{o,max} = \sum_{i=1}^{n} V_i - (n+1)\, V_d \quad (3)$$

for symmetric topology

$$V_{o,max} = \sum_{i=1}^{n} V_i - (n+2)\, V_d \quad (4)$$

for asymmetric topology

Where V_d is the voltage drop on switch during the conduction mode. The voltage rating of switch is main problem in the multilevel inverter. The PIV (peak inverse voltage) of all power switches can be calculated as:

$$PIV_{(pu)} = 6n - 4 \quad (5)$$

with individual DC source

$$PIV_{(pu)} = 6n - 2 \quad (6)$$

without individual DC source

It is noticeable that asymmetric configuration is also applicable to produce large number of output level without increasing the number of DC voltage sources.

3 Comparison Between Proposed Inverter and Other Multilevel Inverter

The main focus of this paper is reduction of required switches as compared to conventional cascaded multilevel inverter for higher level of stepped output waveform. This will improve the efficiency and reliability of inverters configuration. By using asymmetric topology, the higher number of output voltage is produced with lower number of DC voltage source. However, it makes topologies so difficult to be realized. This problem can be overcome by using equal value of DC voltage sources used in symmetric configuration. Moreover, symmetric multilevel inverter produce less number of output level as compared to asymmetric multilevel inverter.

The comparison between symmetric inverter and conventional inverter is done by considering equal number of DC voltage source. This shows the complete difference as compared with conventional inverter. In 2-levl inverter pulse width modulation technique is generally used to generate output voltage waveform. As a result, it will also produce lower total harmonic distortion.

The comparison of features between multilevel inverter and conventional inverter can be easily understand from below Table 1. It shows that switching frequency of multilevel inverter is less as compared to conventional inverter. Same way it requires less switching stress and switching losses as compared to conventional inverter. Thus efficiency and performance of operation are improved in multilevel inverter as compared to conventional inverter. For application point of view multilevel inverters are used for high voltage level application while conventional inverters are used for low and medium voltage application.

The number of component requirement are also most important point for any configuration. This can be easily understanding from next below Table 2. To generate same levels of output voltage by using same number of DC voltage sources, proposed multilevel inverter uses less power switches as compared to cascaded multilevel inverter. For example, to generate nine level output waveform by using four DC voltage sources, a new symmetric multilevel inverter requires ten power switches.

Features	Multilevel Inverter	Conventional Inverter
Total harmonic distortion	Low	High
Switching frequency	Low	High
Switching losses	Low	High
Switching stresses	Low	High
Voltage level	High	low
High voltage application	Yes	No

TABLE 1: COMPARISON OF FEATURES BETWEEN PROPOSED MULTILEVEL INVERTER AND CASCADED MULTILEVEL INVERTER

Parameters	Proposed multilevel inverter	Cascaded multilevel inverter
Required no of DC voltage sources	n	n
No of power switches	2n+2	4n

No of levels in output waveform	2n+1	2n+1
No of on state switches	n+1	2n
Maximum voltage	nV_{dc}	nV_{dc}
$PIV_{(pu)}$	**$6n-4$**	**$4n$**

TABLE 2: COMPARISON OF POWER COMPONENTS REQUIRED FOR PROPOSED MULTILEVEL INVERTER AND CASCADED MULTILEVEL INVERTER

Moreover, the number of gate driver circuit are less required. The number of on state switches also plays an important part for reduction of voltage drop and conduction losses. The voltage and current rating are also considerable part for application point of view that number of power switches are most important than rating of power switches. Because of more reduction in power components, the total PIV (peak inverse voltage) is increased as compared to cascaded multilevel inverter.

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4 Control Strategy and Switching State

4.1 Control Strategy

As suggested the control strategies of the existing multilevel inverter is quite complex and it is time consuming. Therefore, it is thoughtful process to develop a control strategy which is not complex and time consuming. So as per the mission here the strategy which is employed is very simple and gives same number of output levels like cascaded multilevel inverter. Table 3 defines the control strategy for nine level proposed multilevel inverter. In which, one millisecond time is required for each stepped output voltage level. The below table can also be implemented for eleven level stepped output voltage.

To understand the control strategy, it is required to consider switching state for multilevel configuration. Moreover, "Fig. 2."is considered which presents the switching state of H1 switch for total time period is 20 milliseconds. Here each step is considered for 1 millisecond. The fundamental frequency is assumed to be 50Hz.

4.2 Switching State

Table 4 represents switching principle of nine level new symmetric multilevel inverter. In which ten power switches states are considered to generate nine level stepped output voltage. State 1 represents the on condition of power switch while, state 0 represents the off condition of power switch. It is important to notice that switch transition for each level should be low which means that switch state should be remain in same state as possible or should have less transition.

Stepped output voltage level	Time for each step of level
4v	1ms
3v	1ms
2v	1ms
v	1ms
0	1ms
-v	1ms
-2v	1ms
-3v	1ms
-4v	1ms

TABLE 3 : CONTROL STRATEGY FOR NINE LEVEL PROPOSED MULTILEVEL INVERTER

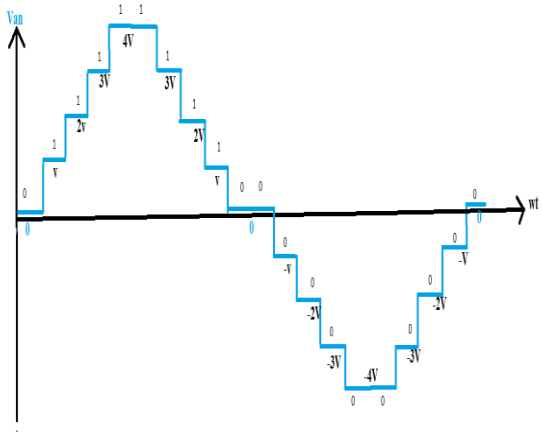

Figure 2: Control strategy for Nine level proposed multilevel inverter

H1 ,H2, H3, H4, H5, H6 switches are considered as a main switches while, S1, S2, S3 and S4 are cosidered as a cell switches. The switches which are used in a common leg shold be in a complementary manner. Thus it will results as a short circuit. Each switches are considered as a bidirectonal switch. So, it will reduce the complexity for any multilevel configuration. Thus symmetric configuration is easy to understand switching state for same value of voltage source.

o/p voltage	H1	H2	H3	H4	H5	H6	S1	S2	S3	S4
4v	1	0	1	0	1	0	1	0	1	0
3v	1	0	0	0	1	1	1	0	1	0
2v	1	0	0	0	1	1	1	0	0	1
v	1	0	0	0	1	1	0	1	0	1
0	0	0	0	1	1	1	0	0	0	0
-v	0	1	1	1	0	0	0	1	0	1
-2v	0	1	1	1	0	0	1	0	0	1
-3v	0	1	1	1	0	0	1	0	1	0
-4v	0	1	0	1	0	1	1	0	1	0

Table 4 : Switching state for 9 level multilevel inverter

5 Simulation Results

To show good performance of the proposed new symmetric multilevel inverter, the simulation results are necessary. Simulated model consists ten IGBT power switches and four equal value of DC voltage sources. The simulation has done by MATLAB/Simulink software. The simulation results are shown here for both symmetric and asymmetric configurations.

"Fig. 3." shows FFT window for voltage and FFT analysis for nine level symmetric multilevel configuration "Fig.4." shows FFT window for voltage waveform and FFT analysis for nine level asymmetric multilevel configuration." Fig.5." shows FFT window for voltage waveform and FFT analysis for fifteen level symmetric multilevel configuration." Fig.6." shows FFT window for voltage waveform and FFT analysis for fifteen level asymmetric multilevel configuration.

As it can be seen, the provided results show that symmetric configuration has less total harmonic distortion as compared to asymmetric configuration. Moreover, it can be also seen that if the number of levels are increased, the total harmonic distortion is decreased.

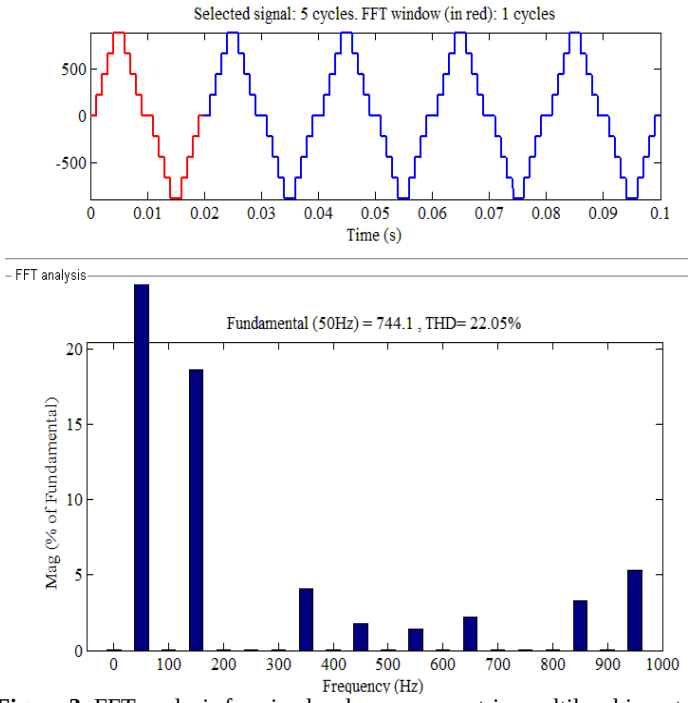

Figure 3: FFT analysis for nine level new symmetric multilevel inverter

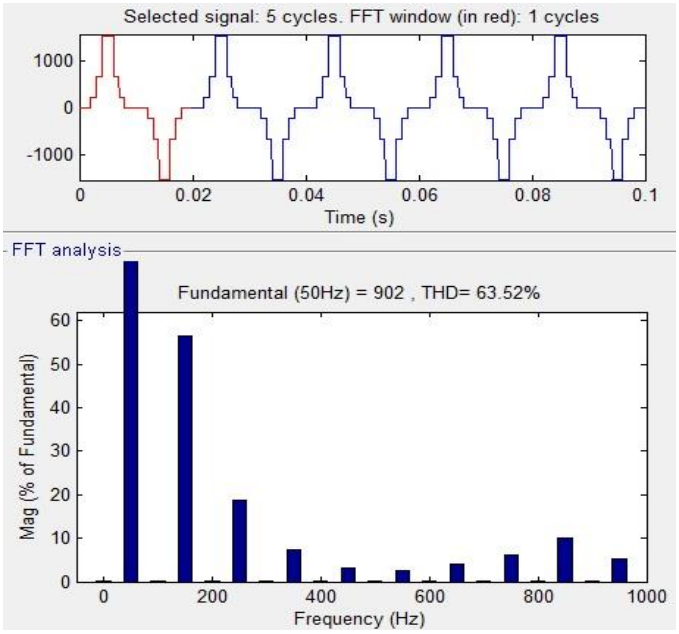

Figure.4: FFT analysis for nine level new asymmetric multilevel inverter

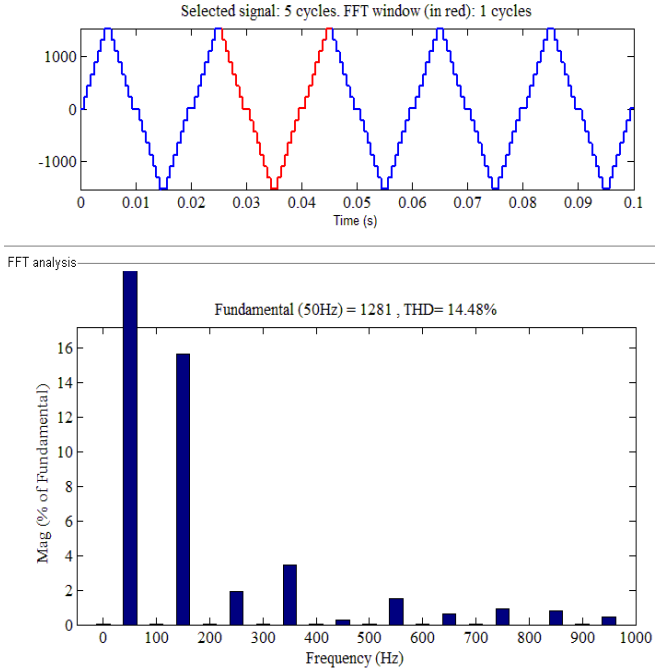

Figure 5: FFT analysis for fifteen level new symmetric multilevel inverter

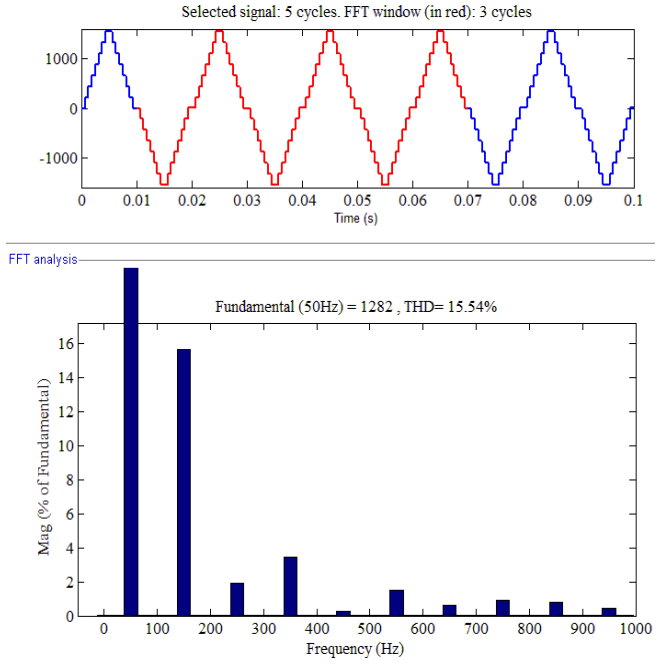

Figure 6 : FFT analysis for fifteen level new asymmetric multilevel inverter

Table 5: Comparison of total harmonic distortion between nine level and fifteen level inverter

Parameter	Symmetric multilevel inverter		Asymmetric multilevel inverter	
No of level	9-level	15-level	9-level	15-level
% THD	22.05	14.48	63.52	15.54

Table 5 represents comparison of total harmonic distortion between 9-levels and 15-level inverter. 9 level new symmetric inverter has low harmonic distortion as compared to 9-level asymmetric inverter. Same way it also differentiates the simulation results for 15-level inverter topology which shows less harmonic distortion even with 9-level new symmetric topology.

6 Conclusion

In this paper, a new symmetric multilevel voltage source configuration with least number of switches is discussed. Moreover, it can be also applicable for asymmetric multilevel configuration. The new symmetric topology consists less number of power switches and gate driver circuit which will improve system performance like efficiency and reliability. A new control strategy can be implemented for new symmetric multilevel inverter by using microcontroller kit based concept. This configuration has low total harmonic distortion compared to other multilevel configuration. It can be concluded that increment in the number of levels reduces total harmonic distortion. Thus, finally comparison of total harmonic distortion can be done by using simulation results.

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