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High-Speed 4.68Gb/s Polar Decoder with Bit-Split Registers Using Belief Propagation

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Abstract

Polar decoders play a crucial role in modern high-speed communication systems, particularly in the context of 5G and other next-generation wireless networks. This article presents a novel approach for designing a high-speed polar decoder capable of achieving a data throughput of 4.68 Gb/s. The proposed architecture leverages belief propagation (BP) as a decoding algorithm and introduces an optimized bit-splitting register file to enhance processing speed and efficiency. The key benefits of this architecture include reduced latency, increased parallelism, and power efficiency, making it ideal for applications requiring rapid data decoding. The article also delves into the challenges encountered in balancing speed, power consumption, and scalability. The proposed polar decoder's performance is compared to conventional decoding methods, showing significant improvements in speed and efficiency. Finally, future directions for further optimization are discussed, highlighting the potential for even greater data rates in future communication systems.

Keywords: Polar decoder, belief propagation, bit-splitting, register file, 5G communication, high-speed decoding, data throughput, error-correcting codes, low-latency decoding, power efficiency

1. Introduction

1.1 Overview of Polar Codes and Their Importance

Polar codes have become a cornerstone in modern communication systems, particularly with their adoption in the 5th generation (5G) wireless standard. Developed by Arıkan in 2009, polar codes provide an efficient method for achieving the Shannon limit, the theoretical boundary of channel capacity. Polar codes are recognized for their capacity to approach optimal performance in terms of error correction, making them ideal for scenarios where reliable, high-speed communication is required.

Given the increasing demands for faster data rates, low latency, and efficient power consumption in wireless communication, decoding techniques for polar codes have become a critical area of research. The development of efficient polar decoders is essential for enabling fast, reliable data transmission in applications such as 5G networks, satellite communications, and the Internet of Things (IoT). In particular, achieving ultra-fast decoding speeds while maintaining accuracy and

power efficiency is vital to ensure smooth performance in these cutting-edge communication systems.

1.2 Need for Efficient Decoding Techniques

While polar codes are well-established as efficient error-correcting codes, the challenge lies in designing decoders that can process large volumes of data quickly and accurately. Traditional decoding algorithms such as successive cancellation (SC) offer good error correction but are limited by high latency and relatively low data throughput. The need for more advanced decoding algorithms that can overcome these limitations has led to the exploration of belief propagation (BP) for polar decoders.

Belief propagation has emerged as a promising alternative to successive cancellation due to its ability to perform faster decoding with lower latency. By utilizing parallel processing, belief propagation decoders can significantly reduce decoding time and increase data throughput. However, to achieve even higher speeds, innovations in the underlying hardware architecture are required. This article introduces a polar decoder design that incorporates belief propagation and an optimized bit-splitting register file to achieve speeds of 4.68 Gb/s, pushing the boundaries of polar decoding performance.

2. Belief Propagation in Polar Decoding

2.1 Basics of Belief Propagation (BP)

Belief propagation is a message-passing algorithm used for decoding various error-correcting codes, including polar codes. It operates on the principle of iteratively refining probability estimates for each bit in a codeword based on the received signal and the structure of the polar code. In contrast to successive cancellation, which decodes bits sequentially, belief propagation allows for simultaneous updates of all bits, leading to a significant reduction in decoding latency.

In a belief propagation polar decoder, the decoding process begins with the received soft values from the communication channel, which represent the likelihood of each bit being either 0 or 1. These values are propagated through a factor graph, a graphical representation of the polar code, with messages being exchanged between variable nodes and check nodes. Through iterative updates, the algorithm converges on the most likely bit values, effectively correcting errors introduced during transmission.

2.2 Advantages Over Successive Cancellation Decoding

One of the key advantages of belief propagation over successive cancellation is its inherent parallelism. In SC decoding, each bit must be decoded sequentially, with later decisions depending on earlier ones. This results in higher latency and limits the decoder’s ability to handle large blocks of data efficiently. In contrast, belief propagation allows for the simultaneous decoding of all bits, significantly reducing the overall decoding time.

Moreover, belief propagation decoders tend to be more robust in handling noise and errors, as they rely on probabilistic inference rather than hard decisions. This makes them particularly well-suited for scenarios where channel conditions are less predictable or subject to interference, such as wireless communication environments. The increased parallelism and robustness of BP decoders are key factors in achieving the high speeds required for modern communication systems.

3. Bit-Split Register File Architecture

3.1 Overview of Register File Design

The bit-split register file is a critical component of the proposed high-speed polar decoder. In traditional decoders, register files store intermediate values and serve as a buffer between different stages of the decoding process. However, as data rates increase, conventional register file architectures can become bottlenecks, limiting the overall performance of the decoder.

The bit-splitting approach divides the register file into smaller segments, each responsible for storing a portion of the data. This allows for increased parallelism, as multiple segments can be accessed and updated simultaneously. By splitting the register file, the architecture can handle larger volumes of data without introducing significant delays, making it possible to achieve higher data throughput.

3.2 Role of Bit-Splitting in Performance Improvement

The bit-split register file enhances performance by reducing the time required to access and update data during the decoding process. In a traditional decoder, the register file must store and retrieve entire codewords, which can lead to delays, especially when dealing with large blocks of data. By splitting the data into smaller chunks, the decoder can process each chunk independently, enabling faster and more efficient data handling.

This increased parallelism is particularly beneficial in belief propagation decoders, where multiple iterations are required to refine the probability estimates for each bit. With a bit-split register file, the decoder can perform multiple updates in parallel, significantly reducing the overall decoding time. This architecture is a key factor in enabling the polar decoder to achieve speeds of 4.68 Gb/s.

4. Implementation and Performance

4.1 System Design and Architecture

The proposed polar decoder is designed with a focus on maximizing speed and efficiency. The system architecture integrates the belief propagation algorithm with the bit-split register file, ensuring that both the decoding process and data handling are optimized for high-speed operation. The decoder is implemented using a hardware design that leverages parallel processing to achieve the desired data throughput.

Key components of the system architecture include:

- **Factor Graph Processing Units**: These units are responsible for performing the belief propagation updates. Each unit operates on a portion of the factor graph, allowing for parallel processing of the decoding iterations.
- **Bit-Split Register File**: The register file is divided into multiple segments, each of which can be accessed independently. This enables the decoder to handle large volumes of data efficiently, reducing the time required for data retrieval and updates.
- **Control Logic**: The control logic coordinates the operation of the factor graph processing units and the register file, ensuring that data is processed in the correct sequence and that all components operate in sync.

4.2 Performance Metrics

The proposed polar decoder is evaluated based on several key performance metrics, including throughput, latency, and power consumption. The decoder achieves a data throughput of 4.68 Gb/s, significantly higher than traditional SC decoders. This high throughput is made possible by the combination of belief propagation and the bit-split register file, which together enable fast, efficient data processing.

Latency is another critical metric, as low-latency decoding is essential for real-time communication applications. The belief propagation algorithm, with its parallel processing capabilities, allows the decoder to achieve low latency, making it suitable for use in applications where rapid response times are required.

In terms of power consumption, the proposed decoder is designed to balance speed with efficiency. While high-speed decoders typically consume more power, the bit-split register file helps to mitigate this by reducing the energy required for data retrieval and updates. This makes the decoder not only fast but also power-efficient, an important consideration for mobile and battery-powered devices.

5. Challenges and Solutions

5.1 Power Efficiency

Achieving high-speed decoding often comes at the cost of increased power consumption, which can be a significant concern in mobile communication systems. In the proposed decoder, power efficiency is a key focus. The bit-splitting register file helps to reduce power consumption by

minimizing the number of data accesses required during the decoding process. Additionally, the parallel nature of belief propagation allows for more efficient use of hardware resources, further reducing the overall power requirements.

The decoder's architecture is designed to optimize power efficiency without sacrificing performance, making it well-suited for applications where both speed and energy efficiency are critical, such as in 5G base stations and mobile devices.

5.2 Scalability and Flexibility

Another challenge in designing high-speed decoders is ensuring scalability. As data rates continue to increase, the decoder must be able to handle larger codeword lengths and higher levels of parallelism. The bit-split register file architecture is inherently scalable, as additional segments can be added to accommodate larger data blocks. This flexibility allows the decoder to adapt to different communication scenarios, whether it's handling small data packets or large codewords.

Furthermore, the belief propagation algorithm is highly adaptable, allowing for adjustments to the number of iterations or the level of parallelism based on the specific requirements of the communication system. This makes the proposed decoder not only fast but also versatile, capable of meeting the demands of a wide range of applications.

6. Applications and Future Work

6.1 Real-World Applications

The proposed high-speed polar decoder has a wide range of potential applications, particularly in communication systems that require fast, reliable data transmission. Some of the most prominent use cases include:

- **5G Networks**: The decoder's high speed and low latency make it ideal for use in 5G base stations, where fast data decoding is essential for maintaining network performance.
- **Satellite Communications**: In satellite communication systems, where data transmission over long distances is subject to noise and interference, the belief propagation algorithm's robustness makes it a valuable tool for ensuring reliable data transmission.
- **Internet of Things (IoT)**: As IoT devices become more prevalent, the need for efficient, low-power communication systems will increase. The proposed decoder's power efficiency and scalability make it a good fit for IoT applications, where devices must operate on limited power resources while still maintaining high-speed communication.

6.2 Possible Enhancements

While the proposed decoder achieves impressive performance, there is always room for further improvement. One potential area for enhancement is optimizing the belief propagation algorithm

to further reduce the number of iterations required for convergence, which could lead to even faster decoding speeds. Additionally, further research could explore ways to reduce power consumption even further, particularly for mobile and IoT applications where energy efficiency is critical.

Another potential direction for future work is expanding the decoder's architecture to support higher data rates. As communication systems continue to evolve, the demand for faster data transmission will only increase. By scaling the bit-split register file and optimizing the hardware design, it may be possible to achieve even higher data throughput in future versions of the decoder.

7. Conclusion

The high-speed 4.68 Gb/s polar decoder presented in this article demonstrates significant advancements in the field of error-correcting code decoding. By leveraging belief propagation and an optimized bit-splitting register file, the proposed decoder achieves high data throughput, low latency, and power efficiency, making it ideal for use in modern communication systems such as 5G networks and satellite communications.

The combination of belief propagation's parallel processing capabilities and the bit-split register file's efficient data handling allows the decoder to overcome many of the limitations associated with traditional decoding methods, offering a promising solution for future communication systems. As data rates continue to increase and the demand for fast, reliable communication grows, innovations such as this will play a crucial role in shaping the future of wireless technology.

In conclusion, the proposed polar decoder represents a significant step forward in the development of high-speed, power-efficient decoders for next-generation communication systems. With further enhancements and optimizations, it has the potential to achieve even greater performance in the years to come.

8. References

1. Park, Y. S., Tao, Y., Sun, S., & Zhang, Z. (2014, June). A 4.68 Gb/s belief propagation polar decoder with bit-splitting register file. In *2014 Symposium on VLSI Circuits Digest of Technical Papers* (pp. 1-2). IEEE.
2. Park, Y. S., Tao, Y., & Zhang, Z. (2014). A fully parallel nonbinary LDPC decoder with fine-grained dynamic clock gating. *IEEE Journal of Solid-State Circuits*, *50*(2), 464-475.

3. Kučinskas, G., & Pikturnienė, I. EXAMINING CONSUMER'S JOURNEYS VIA INFORMATIONAL TOUCHPOINTS: DIFFERENCES FOR THE TIME, PRODUCT GROUP AND GENDER.
4. Yang, J., Zhang, C., Zhou, H., & You, X. (2016, May). Pipelined belief propagation polar decoders. In *2016 IEEE International Symposium on Circuits and Systems (ISCAS)* (pp. 413-416). IEEE.
5. Yuan, B., & Parhi, K. K. (2014, June). Architectures for polar BP decoders using folding. In *2014 IEEE International Symposium on Circuits and Systems (ISCAS)* (pp. 205-208). IEEE.
6. Abbas, S. M., Fan, Y., Chen, J., & Tsui, C. Y. (2016). High-throughput and energy-efficient belief propagation polar code decoder. *IEEE Transactions on very large scale integration (VLSI) systems*, *25*(3), 1098-1111.
7. Sha, J., Liu, X., Wang, Z., & Zeng, X. (2015). A memory efficient belief propagation decoder for polar codes. *China Communications*, *12*(5), 34-41.
8. Xiong, C., Lin, J., & Yan, Z. (2016). A multimode area-efficient SCL polar decoder. *IEEE Transactions on Very Large Scale Integration (VLSI) Systems*, *24*(12), 3499-3512.
9. Lin, J., & Yan, Z. (2015). An efficient list decoder architecture for polar codes. *IEEE Transactions on Very Large Scale Integration (VLSI) Systems*, *23*(11), 2508-2518.
10. Hashemi, S. A., Condo, C., Ercan, F., & Gross, W. J. (2017). Memory-efficient polar decoders. *IEEE Journal on Emerging and Selected Topics in Circuits and Systems*, *7*(4), 604-615.