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Abstract. This paper presents a 4-bit Baugh Wooley multiplier using Full Swing GDI (Gate Diffusion Input) Technology. In general, addition is a crucial arithmetic operation and is heavily demanded in VLSI design. These are widely used in digital signal processing, accumulators, microprocessors and many other applications. So, the full adder performance decides the overall system performance. Proposed design reduces the area as it contains a smaller number of transistors compared to other logic designs.

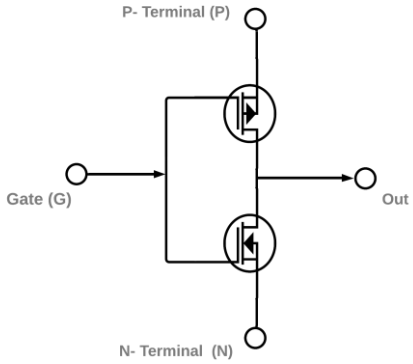
Key Words: *GDI, XOR-XNOR, Full Adder, Full Swing*

INTRODUCTION

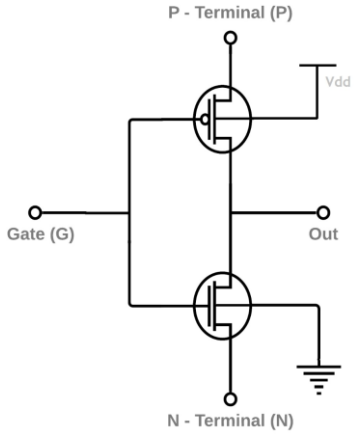
Due to heavy demand in VLSI and area and power are the vital factors in chip design. Now a days almost in every application like mobiles, televisions and in many electronic gadget's chips are the fundamental elements. Full adder is the basic operation in many designs. So, if we improve the performance of full adder automatically performance of the design increases. Here in this paper, we are designing a full adder using full swing GDI Technique which consumes less power and less area. And using that full adder we designed a 4-bit Baugh wooley multiplier. It also consumes lesser area and low power consumption.

GDI (Gate Diffusion Input) Technique

It is an alternative to complementary metal oxide semiconductor (CMOS) Technology. In GDI technique designs consume low power and low area. Here we use a smaller number of transistors compared to CMOS technology, so that we can reduce the area required for the design. Using GDI technique we can calculate complex functions by just using 2 transistors. The basic GDI cell consists of 2 transistors in which we apply supply voltages to gate and P and N shown in the figure below.



In general, GDI cell we connect bulks of PMOS and NMOS to their respective source terminals. In modified GDI structure we connect bulks of PMOS and NMOS to V_{dd} and ground respectively. Modified GDI structure is shown below.



BASIC GDI FUNCTIONS

We can obtain the following Boolean functions using the basic GDI cell as shown in the table below.

N	***P***	***G***	***Out***	***Function***

0	*B*	*A*	*A′B*	*F1*
B	*1*	*A*	*A′+B*	*F2*
1	*B*	*A*	*A+B*	*OR*
B	*0*	*A*	*AB*	*AND*
C	*B*	*A*	*A′B+AB′*	*MUX*
0	*1*	*A*	*A′*	*NOT*
B′	*B*	*A*	*A′B+AB′*	*XOR*
B	*B′*	*A*	*A′B′+AB*	*XNOR*

Above table shows the various logic functions which can be obtained using just 2 transistors. In conventional CMOS design these logic functions require about 6 to12 transistors. These functions are obtained by just interchanging the inputs between input terminals. In the above table f1 and f2 can be called as universal functions for GDI technique just like NAND and NOR gates in CMOS technology. Using f1 and f2 we can realize almost every design using GDI technique.

This technique suits best for manufacturing in twin well CMOS process and SOI silicon on insulator process only as these styles when used with this technique gives less propagation delay and consumes less power.

The GDI cell structure is not the same as the overall PTL techniques and it has some extraordinary highlights. These features allow improvements in designing a complex circuit easily. These improvements include transistor count reduction, low power dissipation. To understand the GDI cell properties analysis of basic cell in different cases and configurations are to be done.

ANALYSIS OF GDI TECHNIQUE

The common problem in PTL is its low swing output signals. It is due to threshold drop across single channel pass transistors. To overcome this problem the PTL that are using at current days uses additional circuitry. In the same way general GDI designs also give low swing output signals, to get the full swing we add extra transistor to the existing design. Although number of transistors are increasing, we are getting full swing output. This increase in number of transistors is also less than actual transistors count in CMOS designs. To comprehend the low swing issue in GDI technique we consider a single function F1 and in the same way It applies to all designs that are designed in GDI technique. In the function F1 low swing occurs when A=0 and B=0. At this input voltage levels the voltage of F1 is V_{tp} rather than 0. This is due to the PMOS pass transistor's poor high-to-low transition. A=0, B=VDD to A=0, B=0 is the only situation where the effect happens in all transformations.

The GDI cell operates as a regular CMOS inverter in about 50% of the cases (for B=1) which is widely used as digital buffer for logic level restoration.

MODIFIED GDI TECHNIQUE

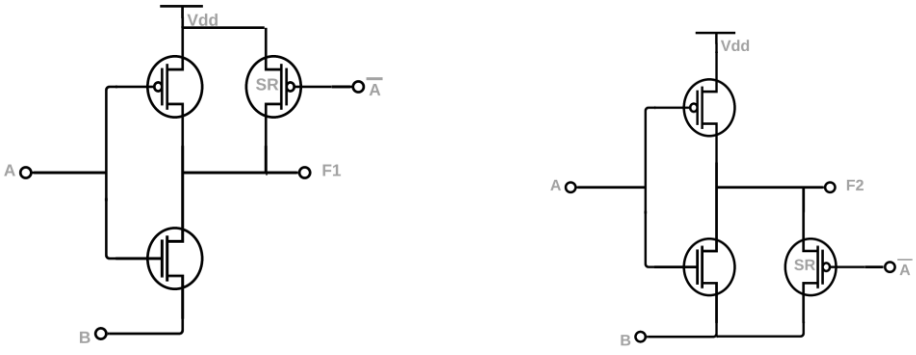
This modification involves adding an extra transistor at the output which restores the swing.

As compared to simple GDI logic, this technique improves the output voltage, control, and power delay product. This logic style can be produced using a regular CMOS process.

Using the full swing GDI technique, the threshold problem was solved and the performance swings degradation was improved.

This new technique only involves in increases in only one transistor, although it increases the overall transistor count, this count is less than the transistors used in complementary metal oxide semiconductor technology.

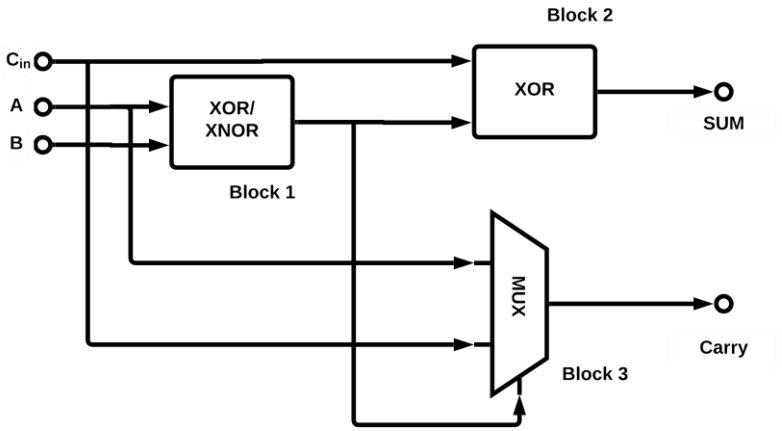
F1 and F2 functions using full swing gdi technique are shown below.



These logic functions produce full swing performance, use less power, are energy efficient, and take up a limited amount of space.

FULL ADDER

Full adder is a basic functional block in many applications. A full adder circuit consists of 3 inputs (A, B, C) and 2 outputs (SUM, CARRY). It is a combinational circuit which perform various 3-bit operations. To design a full adder XOR, XNOR gates and multiplexer are required. So here to design the full adder using GDI technique first we designed the XOR and XNOR gates in GDI technique. The XOR and XNOR signals, as well as their complement signals, determine the overall power consumption and propagation delay of the complete adder.

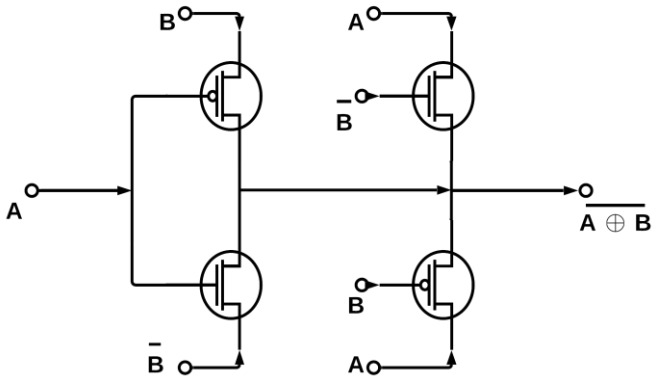


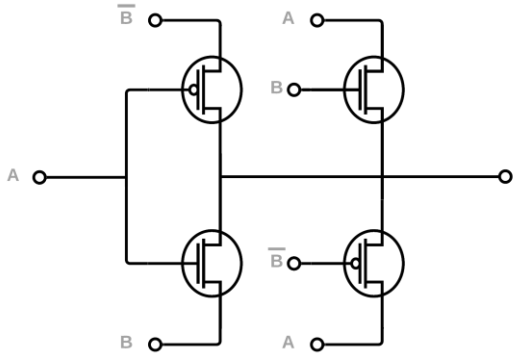
XOR and XNOR GATE

The XOR gate is the basic functional gate in many applications like adder, multiplier, comparator etc., The expression of XOR function is given below

$$A \oplus B = A'B + AB'$$

In the proposed XOR circuit we use 4 transistors



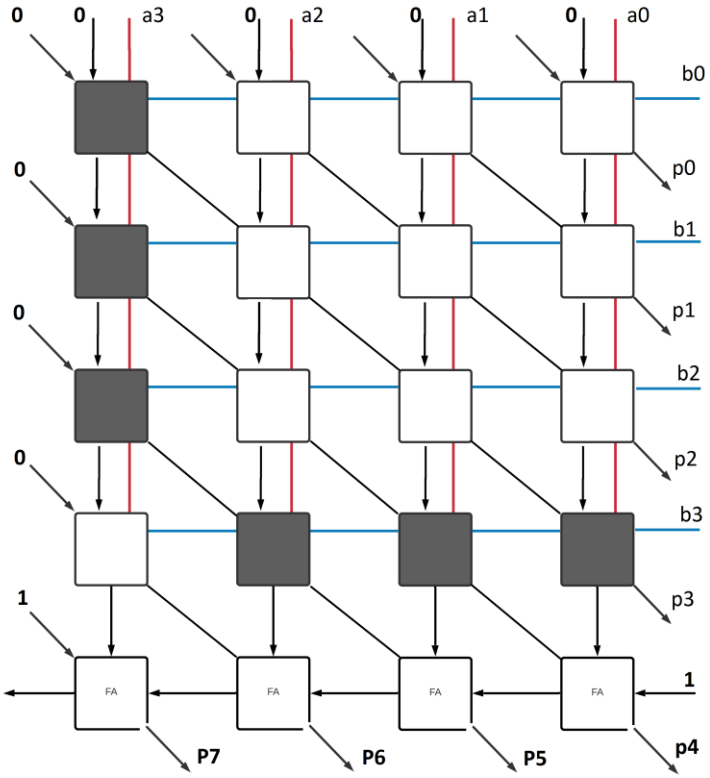


There are 18 transistors in the complete adder that was constructed using full swing gate diffusion input technique. Our design consumes less power compared to the conventional CMOS full adder which constitutes 28 transistors. Our design takes less area as it contains less number of transistors. So the designed full adder is area efficient and power efficient full adder.

Full adder circuit is shown below

MULTIPLIER

Multiplier is a 4-bit 2 input device. The output of the multiplier gives multiplied value of given inputs in binary form. There are different types of multipliers. The proposed design is a 4-bit Baugh Wooley multiplier using full swing gdi technique. We designed the multiplier as shown in the figure below. It is little different from the conventional Baugh wooley multiplier . It contains more number of full adders when compared to general one. The discussed design consists of two types of cells ,they are grey and white cells. A complete adder and a Nand gate are attached to the grey cell. A complete adder and a and gate are attached to the white cell. The whole structure gives outputs p1 to p8. These p1 to p8 are the output bits of multiplied value. In this designed multiplier the power consumption is more compared to the base paper because the design of multiplier we used contains more number of full adders compared to the referenced one. It contains total 20 full adders internal which functions parallelly. Our design constitutes less area as it contains less number of transistors in total. As every basic component of this multiplier is designed using gdi technique, each one takes take less number of transistors which in total reduces the transistor count.



The power and delay results are shown in below table.

RESULTS AND COMPARISONS

As the multiplier is designed using GDI technique instead of CMOS technology, number of transistors used to design the multiplier were reduced and power consumption also reduced. The power calculated for the designed full adder was 211.7E-9W. This power was very less compared to full adder designed in CMOS technology. When we put together this full adder and combine them into a multiplier, we get the power high power as we are combining total of 20

full adders which are internally structured in grey and white cells. As these cells are combined parallelly, the power consumption is little higher.

CONCLUSION

The designed Baugh Wooley multiplier using GDI technique is consuming less powe and less area as compared to others technologies. The out of this multiplier is also full swing output.

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